ABSTRACT

In a PLL circuit, the number of LPFs is reduced to one to reduce mounting area and pin number, and to simplify design. In one embodiment, the PLL circuit includes a variable-gain phase comparator, a mixer, an LPF, VCOs, couplers, and a control circuit to controlling the on/off operation of the VCOs. The variable-gain phase comparator is capable of varying a phase difference gain. The on/off of the operation of the VCOs is controlled by the control circuit so that one of the VCOs is turned off. The phase difference conversion gain is varied in accordance with the sensitivity of the VCOs so the number of LPFs required for the PLL circuit can be reduced to only one.